2020-April

DIM-335x
Hardware User Manual

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Revision History

Version	Date	Description
V1.0	2020-April	First release

Table of Contents

1 Introduction

DIM-335x is a highly configurable, small form-factor processor cards features one of Texas Instruments Sitara AM335x Processors. The module includes DDR3 RAM memory and NAND FLASH or eMMC subsystems. DIM-335x provides a complete and flexible CPU infrastructure for highly integrated embedded systems.

The onboard AM335x processor provides Cortex-A8 32-bit RISC processor with a NEON SIMD coprocessor. This MPU is capable of running a rich set of real-time operating systems containing software applications programming interfaces (APIs) expected by modern system designers. The ARM architecture supports several operating systems, including Linux, QNX, and Windows CE.

2 Overview

2.1 Features

- Texas Instruments Cortex-A8 Sitara AM335x SoC,up to 1GHz
- Up to 1GB DDR3
- Up to 1GB NAND or up to 8GB eMMC memory option
- SPI NOR Flash
- CRYPTO or EEPROM
- Display controller with support of up to WXGA (1366 x 768) resolution
- PowerVR SGX GPU with OpenGL-ES and OpenVG support
- Gigabit Ethernet, USB2.0x2, UARTx6, GPIOx65, SDIOx3, SPIx2, I^2Cx3, CAN,ADC
- Linux, Windows Embedded Compact 7
- Tiny size: 67.60x38.02x5 mm
- Evaluation Board:EVB-D335

2.2 Block Diagram

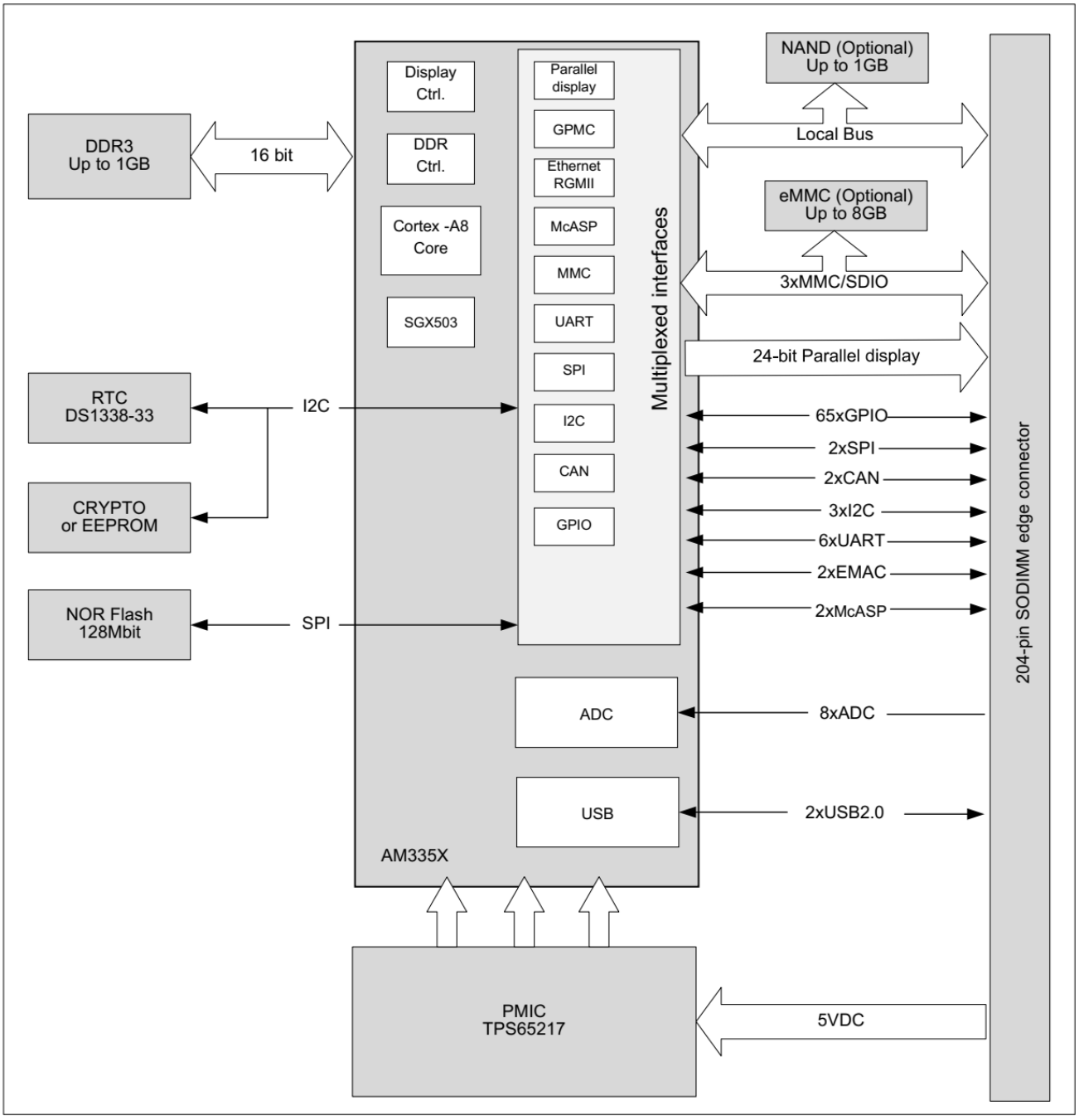

Figure 1 DIM-335x Block Diagram

2.3 DIM-335x Features

Table 1 System and Graphics

Feature	Specifications
CPU	TI ARM Cortex-A8 processor AM335x, up to 1GHz 32KB (L1) + 256KB (L2) cache
RAM	Up to 1GB, DDR3, 16-bit bus width
Memory	On-board NAND flash or eMMC option： NAND flash up to1GB, 8bit, SLC eMMC up to 8GB,8bit
	On-board NOR flash:16MB,SPI
	On-board CRYPTO or EEPROM optional
Graphics Acceleration Unit	PowerVR SGX530 GPU providing 2D/3D graphics acceleration with OpenGL-ES and OpenVG support.

Table 2 Peripherals Interface

Feature	Specifications
Display	Parallel 24-bit display interface - up to 1366 x 768
USB	2 OTG USB2.0 high-speed ports, 480 Mbps
UART	Up to 6 UART ports
CAN bus	Up to 2 CAN bus interfaces, 3.3V levels
MMC / SDIO	Up to 3 MMC/SD/SDIO interfaces, support for HC MMC and SDHC up to 32GB
I2C	Up to 3 I2C interfaces (up to 400Kbps)
SPI	Up to 2 configurable SPI bus interfaces (Slave/Master modes)
General Purpose IO	Up to 65 multifunction signals. Can be used as GPIO (shared with other functions)
Audio	Up to Two Multichannel Audio Serial Ports(McASPs)
ADC	Up to 8 general-purpose ADC channels
RTC	Real time clock, powered by external lithium battery
Gigabit Ethernet	Up to Two Industrial Gigabit Ethernet MACs (10,100, 1000 Mbps)
Touch-screen	4/5/8-wire resistive touch-screen support

Table 3 Electrical, Mechanical and Environmental Specifications

Feature	Specifications
Supply Voltage	5V DC main power supply
Active power consumption	Depending on board configuration, CPU speed and system load.
Dimensions	67.60 x38.02x5 mm
Operation temperature (case)	Commercial: 0 to70℃ Extended: -20 to 70 ℃ Industrial: -40 to 85 ℃
Storage temperature	-40 to 85 ℃
Relative humidity	10% to 90% (operation) 05% to 95% (storage)
Connectors	204-pin SODIMM edge connector

3 Core System Components

3.1 AM335x SoC

AM335x SoC manufactured by Texas Instruments provides up to 1GHz Sitara ARM Cortex-A8 32-bit RISC CPU. It supports the following main features:

- NEON SIMD Coprocessor
- 32 KB of L1 Data and 32 KB of L1 Instruction Cache
- 256 KB of L2 Cache with ECC
- SGX530 3D Graphics Engine
- Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS)
- USB 2.0 High-Speed OTG port with Integrated PHY
- 10/100/1000 Mbps Ethernet MAC controller

3.2 Graphics Subsystem

The AM335x 2D and 3D graphics accelerator (SGX) provides support for the following imaging and video features:

- 2D and 3D graphics, vector graphics, and programming support for GP-GPU functions
- Tile-based architecture
- An advanced shader feature set in excess of Microsoft VS3.0, PS3.0 and OGL2.0
- Industry standard API supports Direct3D mobile, OGL-ES 1.1 and 2.0, OpenVG 1.0.1 and OpenMax
- Fine-grained task switching, load balancing and power management
- Programmable high-quality image anti-aliasing
- Advanced geometry DMA driven operation for minimum CPU interaction
- Fully virtualized memory addressing for OS operation in a unified memory architecture

3.3 Memory

3.3.1 DDR3 RAM

The AM335x processor includes one dedicated 16 bit DDR SDRAM memory interface.

DIM-335x is equipped with up to 1GB of DDR3 RAM integrated on board the module. The memory bus interface is capable of burst transfer rates of 1200 MB / second.

3.3.2 NAND Flash Option

DIM-335x is equipped with up to 1GB of SLC NAND Flash, which serves as the main non-volatile storage of DIM-335x. This storage is used for storing the system boot-loader and the OS. The NAND Flash memory is connected to the AM335x processor using the general purpose memory controller (GPMC) bus.

The GPMC bus is also accessible on the SO-DIMM-204 connector. It can be used to access external memories such as SDRAM, SRAM, NOR flash, NAND flash, or memory-mapped ASICs and FPGAs. The inteface is a maximum of 16-bits wide, but can also be used for 8-bit access.

3.3.3 eMMC Option

DIM-335x also can be equipped with up to 32GB eMMC instead of NAND Flash. The eMMC is connected to the AM335x processor through 8-bit MMC1 port.

AM335x processor provides up to three MMC, SD, SDIO Ports,Data Transfer Rate up to 48-MHz.

3.3.4 NOR Flash

Up to 16 MB of on-board NOR Flash memory is connected to the AM335x using the Serial Peripheral Interface 0 (SPI0). The AM335x provides up to 2 SPI interfaces with both interfaces available on the SO-DIMM connector.

3.3.5 CRYPTO or EEPROM (Optional)

The DIM-335x contains a CryptoAuthentication that is used to hold configuration data for the module. The CryptoAuthentication is connected to the AM335x using the I2C0 interface.If do not want Crypto Element on the module,it is also can choose the EEPROM configuration instead.

4 Peripheral Interfaces

4.1 LCD Interface

The DIM-335x display subsystem is implemented with the AM335x LCD controller:

- 16-bits data output (RGB565)
- Resolution up to 1366 x 768 (with maximum 126-MHz pixel clock)
- Integrated LCD interface display driver (LIDD) controller
- Integrated DMA engine to pull data from the external frame buffer without burdening the processor via interrupts or a firmware timer
- Supported display types:
  - Character displays - uses LCD interface display driver (LIDD) controller to program these displays
  - Passive matrix LCD displays - uses LCD raster display controller to provide timing and data for constant graphics refresh to a passive display
  - Graphics refresh to a passive display external frame buffer space and the Internal DMA engine to drive streaming data to the panel

For more information about display operating modes refer to chapter 13 of the " AM335x Technical Reference Manual " .

The LCD interface signals of DIM-335x are detailed in Table 4.

Table 4 LCD Interface signals

Signal Name	Pin Number	Description	At 16bit mode color map
LCD interface			
LCD_DATA0	Pin29	Pixel data bit 0	B0
LCD_DATA1	Pin31	Pixel data bit 1	B1
LCD_DATA2	Pin33	Pixel data bit 2	B2
LCD_DATA3	Pin35	Pixel data bit 3	B3
LCD_DATA4	Pin39	Pixel data bit 4	B4
LCD_DATA5	Pin41	Pixel data bit 5	G0
LCD_DATA6	Pin43	Pixel data bit 6	G1
LCD_DATA7	Pin45	Pixel data bit 7	G2
LCD_DATA8	Pin47	Pixel data bit 8	G3
LCD_DATA9	Pin49	Pixel data bit 9	G4
LCD_DATA10	Pin51	Pixel data bit 10	G5
LCD_DATA11	Pin53	Pixel data bit 11	R0
LCD_DATA12	Pin57	Pixel data bit 12	R1
LCD_DATA13	Pin59	Pixel data bit 13	R2
LCD_DATA14	Pin61	Pixel data bit 14	R3
LCD_DATA15	Pin63	Pixel data bit 15	R4
LCD_PCLK	Pin65	Pixel clock	
LCD_VSYNC	Pin67	Vertical synchronization	
LCD_HSYNC	Pin69	Horizontal synchronization	
LCD_BIAS_EN	Pin71	Data validation/blank,data enable	

NOTE: 1. LCD_DATA[0:15] lines function as SYSBOOT inputs at PWRONRSTn rising edge. Therefore these pins must not be driven by the evaluation board during the DIM-335x boot process.

2. If want to display in 24-bits data output,please refer the pin attributes at chapter 7.1 and get the information about the pin assignment of LCD_DATA[16:23].It is also can refer the design on Evaluation Board EVB-D335.

4.2 USB

The DIM-335x USB ports are implemented with the AM335x USB 2.0 OTG controller ,including USB0 and USB1.The interfaces provide the following features:

- Supports USB 2.0 High Speed (480Mbps), Full Speed (12Mbps) and Low Speed (1.5Mbps) operation in host mode
- Supports USB 2.0 High Speed (480 Mbps) and Full Speed (12 Mbps) operation in peripheral mode.
- Supports USB OTG extensions for Session Resume Protocol (SRP) and Host Negotiation Protocol (HNP).

USB interface signals of DIM-335x are detailed in Table 5 and Table 6.

Table 5 USB0 Interface signals

Signal Name	Pin Number	Description
USB0_VBUS	Pin115	USB0_VBUS. This pin must be connected to the 5V VBUS rail.
USB0_ID	Pin117	USB0 ID signal
USB0_DN	Pin131	USB0 negative data
USB0_DP	Pin133	USB0 positive data
USB0_CE	Pin135	USB0 Active high Charger Enable output
USB0_DRVVBUS	Pin139	USB0 active high VBUS control output

Table 6 USB1 Interface signals

Signal Name	Pin Number	Description
USB1_VBUS	Pin119	USB1_VBUS. This pin must be connected to the 5V VBUS rail.
USB1_ID	Pin129	USB1 ID signal
USB1_DN	Pin123	USB1 negative data
USB1_DP	Pin121	USB1 positive data
USB1_CE	Pin125	USB1 Active high Charger Enable output
USB1_DRVVBUS	Pin137	USB1 active high VBUS control output

4.3 UART

Up to 6 UART ports are available with DIM-335x. All UART ports are derived from the AM335x SoC integrated UARTs and support the following features:

- 16C750 compatibility
- Baud rate from 300 bps up to 3.6864 Mbps
- Auto-baud between 1200 bps and 115.2 Kbps
- IrDA and CIR modes

For additional details, please refer to chapter 19 of the “AM335x Technical Reference Manual”.

The UART signals are detailed in Table 7.

Table 7 UART signals

Signal Name	Pin Number	Description
UARTx_CTSN	Pin*	UART Clear to Send
UARTx_RTSN	Pin*	UART Request to Send
UARTx_RXD	Pin*	UART Receive Data
UARTx_TXD	Pin*	UART Transmit Data

NOTE: Pin* represents multiplexing IO,please refer the pin attributes at chapter 7.1.

4.4 CAN Bus

DIM-335x features two digital CAN bus interfaces. CAN bus interfaces are implemented with the AM335 CAN communication modules. CAN support the following main features:

- CAN protocol version 2.0 part A, B (ISO 11898-1)
- Programmable bit rate up to 1 Mb/sec
- Programmable FIFO mode for message objects

For additional details, please refer to section 23 of the “AM335x Technical Reference Manual”.

The CAN BUS signals are detailed in Table 8.

Table 8 CAN BUS signals

Signal Name	Pin Number	Description
DCANx_TX	Pin*	Transmit Line
DCANx_RX	Pin*	Receive Line

NOTE: Pin* represents multiplexing IO,refer the pin attributes at chapter 7.1.

4.5 MMC/SDIO

The DIM-335x features up-to three multimedia card high-speed/secure data/secure digital IO (MMC / SD / SDIO) host interfaces. Each MMC/SD/SDIO host controller supports a single MMC / SD / SDIO card or device.

The general features of the MMCHS host controller IP are:

- Built-in 1024-byte buffer for read or write
- MMC command/response sets as defined in the MMC standard specification v4.3
- SD command/response sets as defined in the SD Physical Layer specification v2.00
- SDIO command/response sets and interrupt/read-wait suspend-resume operations as defined in the SD part E1 specification v2.00
- Clock support:
  - 96-MHz functional clock source input
  - Up to 384Mbit/sec (48MByte/sec) in MMC mode 8-bit data transfer
  - Up to 192Mbit/sec (24MByte/sec) in High-Speed SD mode 4-bit data transfer
  - Up to 24Mbit/sec (3MByte/sec) in Default SD mode 1-bit data transfer

For additional details, please refer to chapter 18 of the “AM335x Technical Reference Manual”.

The MMC/SDIO interface signals are detailed in Table 9.

Table 9 MMC/SDIO interface signals

Signal Name	Pin Number	Description
MMCx_CLK	Pin*	MMC/SD serial clock output
MMCx_CMD	Pin*	MMC/SD command signal
MMCx_DAT0	Pin*	MMC/SD data signal
MMCx_DAT1	Pin*	MMC/SD data signal, SDIO interrupt input
MMCx_DAT2	Pin*	MMC/SD data signal, SDIO read wait output
MMCx_DAT[7:3]	Pin*	MMC/SD data signals
MMCx_POW	Pin*	MMC/SD power supply control (MMCHS 0 only)
MMCx_SDCD	Pin*	SD card detect (from connector)
MMCx_SDWP	Pin*	SD write protect (from connector)
MMCx_OBI	Pin*	MMC out of band interrupt

NOTE: Pin* represents multiplexing IO,please refer the pin attributes at chapter 7.1.

4.6 I2C

DIM-335x features up-to three general purpose I2C interfaces. The following features are supported:

- Compliance with Philips I2C specification version 2.1
- Multiple-master operation
- Support for standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Arbitration-lost interrupt with automatic mode switching from master to slave

The I2C interfaces are implemented with the AM335 integrated I2C controller. For additional details, please refer to section 21 of the “AM335x Technical Reference Manual”.

The I2C signals are detailed in Table 10.

Table 10 I2C signals

Signal Name	Pin Number	Description
I2Cx_SCL	Pin*	I2C serial clock (open drain)
I2Cx_SDA	Pin*	I2C serial data (open drain)

NOTE: 1. Pin* represents multiplexing IO,refer the pin attributes at chapter 7.1.

2. I2C0 is used on DIM-335x module,and do not supoort through the carrier board interface.

4.7 SPI

DIM-335x features up-to two Enhanced Configurable SPI ports with two chip-select signals each. All CM-T335 SPI ports are derived from the AM335x SoC integrated McSPI IPs. The following main features are supported:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Buffered receive/transmit data register per channel (1 word deep)
- Multiple SPI word access with one channel using a FIFO
- Two DMA requests per channel, one interrupt line

For additional details, please refer to section 24 of the “AM335x Technical Reference Manual”.

The SPI0 signals are detailed in Table 11.

Table 11 SPI0 signals

Signal Name	Pin Number	Description
SPI0_CS0	Pin191	SPI Chip Select
SPI0_CS1	Pin189	SPI Chip Select
SPI0_D0	Pin183	SPI Data
SPI0_D1	Pin185	SPI Data
SPI0_CLK	Pin187	SPI Clock

NOTE: About SPI1 application,refer the pin attributes at chapter 7.1.

4.8 ADC / Touch-Screen

CM-T335 features an ADC module that can act as a resistive touch-screen controller. The interface supports 4/5/8-wire touch panels and is available through the carrier board interface.

The ADC and touch screen signals are detailed in Table 12.

Table 12 ADC and Touch-Screen signals

Signal Name	Pin Number	Description
AIN0	Pin184	Touch screen X- (left) \ Analog Input/Output
AIN1	Pin186	Touch screen X+ (right) \ Analog Input/Output
AIN2	Pin188	Touch screen Y+ (top) \ Analog Input/Output
AIN3	Pin190	Touch screen Y- (bottom) \ Analog Input/Output
AIN4	Pin192	Analog Input/Output
AIN5	Pin194	Analog Input
AIN6	Pin196	Analog Input
AIN7	Pin198	Analog Input

4.9 Audio

DIM-335x features up-to two Multichannel Audio Serial Ports(McASPs),support the following features:

- S/PDIF transmit physical layer components.
- Up to 384 subframes blocks.
- S/PDIF, IEC60958-1, AES-3 formats.
- TDM streams from 2 to 32 time slots.

For additional details, please refer to section 22 of the “AM335x Technical Reference Manual”.

The Audio interface signals are detailed in Table 13.

Table 13 Audio interface signals

Signal Name	Pin Number	Description
McASPx_ACLKR	Pin*	Receive Bit Clock
McASPx _ACLKX	Pin*	Transmit Bit Clock
McASPx _AHCLKR	Pin*	High speed receive clock
McASPx _AHCLKX	Pin*	High speed transmit clock
McASPx _AXR[3:0]	Pin*	Audio transmit/receive pin
McASPx _FSR	Pin*	Receive Frame Sync
McASPx _FSX	Pin*	Transmit Frame Sync

NOTE: Pin* represents multiplexing IO,please refer the pin attributes at chapter 7.1.

4.10 GPIO

The AM335 provides up to 94 GPIO signals. The GPIO subsystem is derived from the AM335 integrated GPIO controller. The AM335 GPIOs are divided into 4 blocks with up to 31 GPIOs in each block. The GPIO signals can be configured for the following applications:

- Data input / output
- Synchronous interrupt generation
- Keyboard interface with a de-bouncing cell
- GPIO0 block can generate a Wake-up request in Idle mode

For additional details, please refer to section 25 of the “AM335x Technical Reference Manual”.

Note: Not all GPIO signals supported by the AM335x SoC are available through the DIM-335x carrier board interface.

4.11 Ethernet

DIM-335x provides up to two Ethernet interfaces. Ethernet interfaces are implemented with the AM335 Industrial Gigabit Ethernet MACs. Ethernet interfaces support the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant
- Integrated Switch
- Each MAC Supports MII, RMII, RGMII, and MDIO Interfaces
- Ethernet MACs and Switch Can Operate Independent of Other Functions

For additional details, please refer to section 14 of the “AM335x Technical Reference Manual”.

The Ethernet interface signals are detailed in Table 14.

Table 14 Ethernet interface signals

Signal Name	Pin Number	Description
GMIIx_RXCLK	Pin*	GMII/MII Receive clock
GMIIx_RXD[3:0]	Pin*	GMII/MII Receive data
GMIIx_RXDV	Pin*	GMII/MII Receive data valid
GMIIx_RXER	Pin*	GMII/MII Receive error
GMIIx_COL	Pin*	GMII/MII Collision detect
GMIIx_CRS	Pin*	GMII/MII Carrier sense
GMIIx_TXCLK	Pin*	GMII/MII Transmit clock
GMIIx_TXD[3:0]	Pin*	GMII/MII Transmit data
GMIIx_TXEN	Pin*	GMII/MII Transmit enable
RGMIIx_RCLK	Pin*	RGMII Receive clock
RGMIIx_RCTL	Pin*	RGMII Receive control
RGMIIx_RD[3:0]	Pin*	RGMII Receive data
RGMIIx_TCLK	Pin*	RGMII Transmit clock
RGMIIx_TCTL	Pin*	RGMII Transmit control
RGMIIx_TD[3:0]	Pin*	RGMII Transmit data
RMIIx_RXD[1:0]	Pin*	RMII Receiver data
RMIIx_RXER	Pin*	RMII Receiver error
RMIIx_CRS_DV	Pin*	RMII Carrier sense / Data valid
RMIIx_TXEN	Pin*	RMII Transmit enable
RMIIx_REFCLK	Pin*	RMII Reference clock
RMIIx_TXD[1:0]	Pin*	RMII Transmit data
MDIO_CLK	Pin*	MDIO Serial clock
MDIO_DATA	Pin*	MDIO Serial data

NOTE: Pin* represents multiplexing IO,please refer the pin attributes at chapter 7.1.

4.12 JTAG

The DIM-335x JTAG interface is supported via the ARM Debug Access Port (DAP) of the AM335x SoC. JTAG IEEE 1149.1, 1149.6 and IEEE 1149.7 JTAG standards are supported.

For additional details, please refer to section 27.1.2 of the “AM335x Technical Reference Manual”.

The JTAG signals are detailed in Table 15.

Table 15 JTAG signals

Signal Name	Pin Number	Description
EMU0	Pin160	Misc Emulation pin
EMU1	Pin162	Misc Emulation pin
TCK	Pin166	JTAG Test Clock
TDI	Pin168	JTAG Test Data input
TDO	Pin170	JTAG Test Data output
TMS	Pin172	JTAG Test Mode Select
TRSTN	Pin174	JTAG Test Reset (active low)

5 System Logic

5.1 Power Management

DIM-335x features a Power Management IC (PMIC) which supports the SoC and the peripheral power rails. The PMIC integrates step down converters, power fail protection and thermal shutdown protection.

The power rails that support the DIM-335x are detailed in Table 16.

Table 16 Power Rails Operating Conditions

Supply Name	Min	Typ.	Max	Unit	Description
VIN_AC	4.3	5.0	5.8	V	Main power supply.Connect this pin to an external DC supply.
VDD_USB	4.3	5.0	5.8	V	USB voltage input to power path. Connect this pin to an external voltage from a USB port.
RTC_VBAT	1.3	3.0	3.7	V	Backup power supply for RTC.
USB_VBUS	0	5.0	5.25	V	Supply voltage for USB VBUS comparator input.

NOTE: VIN_AC,VDD_USB are input to power path of PMIC, and converted to multiple power rails by the PMIC. Refer to EVB-D335 reference design.

5.2 Reset

The reset management of the AM335x SoC is done by the on-chip Power, Reset and Clock Management (PRCM) module. It can receive reset input from several sources, of two types: warm reset and cold reset.

For additional details, please refer to section 8.1.7 of the “AM335x Technical Reference Manual”.

Two of the reset sources for the PRCM module are hardware pins that can be addressed externally to the DIM-335x. Both of the reset signals are active low.

The DIM-335x reset signals are detailed in Table 17.

Table 17 Reset signals

Signal Name	Pin Number	Description
PMIC_NRST	Pin36	Cold reset
AM33_WNRST	Pin158	Warm reset

5.3 Boot Sequence

On startup, at PWRONRSTn reset signal rising edge, the boot sequence is configured according to SYSBOOT inputs. After booting device list creation, the AM335x initiates a booting procedure. If a boot image is found on a

device, the boot code executes. Otherwise, the next boot device enumerated in the list is examined. The device waits for the watchdog to deliver a reset signal and restart the boot procedure.

On the DIM-335x,the SYSBOOT inputs have been tied to the right level,and it can change the boot device through the switch SW1. So there is no need to configure the pins of sysboot on Evaluation Board.

For more information regarding booting, refer to chapter 26.1.6 of the “AM335x Technical Reference Manual”.

Boot Sequence of different configuration on DIM-335x are detailed in Table 18 and Table 19.

Table 18 Boot Sequence of NAND Flash Option

SW1 Switch position	1st	2nd	3rd	4th	Description
2-3	NAND	NANDI2C	MMC0	UART0	NAND Flash (NAND) is the main system boot device
1-2	MMC0	SPI0	UART0	USB0	Change the switch position of SW1,can change the boot device to SDcard (MMC0) or the other

Table 19 Boot Sequence of eMMC Option

SW1 Switch position	1st	2nd	3rd	4th	Description
1-2	MMC1	MMC0	UART0	USB0	eMMC (MMC1) is the main system boot device
2-3	SPI0	MMC0	USB0	UART0	Change the switch position of SW1,can change the boot device to SDcard (MMC0) or the other

NOTE: LCD_DATA[0:15] lines function as SYSBOOT inputs at PWRONRSTn rising edge. Therefore these pins must not be driven by the evaluation board during the DIM-335x boot process. Refer to EVB-D335 reference design.

5.4 RTC

DIM-335x features an on-board low-power DS1338 real time clock (RTC). The RTC is connected to the AM335x SoC using I2C0 interface.

At main power supply absence, in order to maintain activities of the RTC, i.e. clock advancement and data storage, a use of a backup supply is essential. The backup supply may be derived from a super-cap or a battery.

For more information about RTC refer to the DS1338 datasheet.

6 Operational Characteristics

6.1 Absolute Maximum Ratings

The absolute maximum voltage ratings are described in Table 20. Any deviation from the listed values may result in permanent damage to the device. For recommended operating conditions see chapter 6.2.

Table 20 Absolute Maximum ratings

Supply Name	Description	Min	Max	Unit
VIN_AC	Main power supply.Connect this pin to an external DC supply.	-0.3	20	V
VDD_USB	USB voltage input to power path. Connect this pin to an external voltage from a USB port.	-0.3	20	V
RTC_VBAT	Backup power supply for RTC.	-0.3	6	V
USB_VBUS	Supply voltage for USB VBUS comparator input.	-0.5	5.25	V
Voltage at I/O pins	Steady state max voltage at all I/O pins	-0.5	3.3	V
VDD_SYS	System voltage output of PMIC on module	-0.3	7	V
		-	3	A
PMIC_BCG	Battery charger output of PMIC on module	-0.3	7	V
		-	3	A
VIO_3P3	Module power output	1.8	3.3	V
		-	0.4	A

6.2 Recommended Operating Conditions

The recommended operating conditions are described in Table 21.

Table 21 Recommended Operating Conditions

Supply Name	Description	Min	Typ.	Max	Unit
VIN_AC	Main power supply.Connect this pin to an external DC supply.	4.3	5.0	5.8	V
VDD_USB	USB voltage input to power path. Connect this pin to an external voltage from a USB port.	4.3	5.0	5.8	V
RTC_VBAT	Backup power supply for RTC.	1.3	3.0	3.7	V
USB_VBUS	Supply voltage for USB VBUS comparator input.	0	5.0	5.25	V

6.3 IO Electrical Characteristics

The I/O electrical characteristics are described in Table 22.

Table 22 DC Electrical Characteristics for digital IO

Parameter	Description	Min	Max	Unit
V_{IH}	High-level input voltage.	2	3.3	V
V_{IL}	Low-level input voltage.	0	0.8	V
V_{OH}	High-level output voltage.	2.85		V
V_{OL}	Low-level output voltage	0	0.45	V

NOTE: DC electrical characteristics listed above are generic. For specific signals characteristics, refer to AM335x datasheet.

6.4 Operating Temperature Ranges

DIM-335x is available with three options of operating temperature range, which are described in Table 23.

Table 23 DIM-335x Temperature Range Options

Rang	Temperature
Commercial	0 to 70 ℃
Extended	-20 to 70 ℃
Industrial	-40 to 85 ℃

7 SO-DIMM-204 Interface Description

7.1 Pin Attributes

PIN	Class	Signal	PMIC Pin	AM3352 Pin	Domain Power	Option Signal0	Option Signal1	Option Signal2	Option Signal3	Option Signal4	Option Signal5	Option Signal6	Option Signal7
1	PWR	VIN_AC	10	-	-								
2	PWR	GND	-	-	-								
3	PWR	VIN_AC	10	-	-								
4	PWR	GND	-	-	-								
5	PWR	VIN_AC	10	-	-								
6	PWR	GND	-	-	-								
7	PWR	VIN_AC	10	-	-								
8	PWR	GND	-	-	-								
9	PWR	VDD_USB	12	-	-								
10	PWR	GND	-	-	-								
11	PWR	VDD_USB	12	-	-								
12	PWR	GND	-	-	-								
13	PWR	VDD_USB	12	-	-								
14	PWR	GND	-	-	-								
15	PWR	VDD_USB	12	-	-								
16	PWR	GND	-	-	-								
17	PWR	GND	-	-	-								
18	PWR	GND	-	-	-								
19	PWR	GND	-	-	-								
20	PWR	GND	-	-	-								
21	PWR	VDD_SYS	7,8	-	-								
22	PWR	PMIC_BCG	4,5	-	-								
23	PWR	VDD_SYS	7,8	-	-								
24	PWR	PMIC_BCG	4,5	-	-								
25	PWR	VDD_SYS	7,8	-	-								
26	PM	PMIC_BVS	6	-	-								
27	PWR	VDD_SYS	7,8	-	-								
28	PM	PMIC_BTS	11	-	-								
29	335M	LCD_DATA0	-	R1	3.3V	lcd_data0	gpmc_a0	pr1_mii_mt0_clk	ehrpwm2A	pr1_pru1_pru_r30_0	pr1_pru1_pru_r31_0	gpio2_6	
30	PWR	VIO_3P3	-	-	-								
31	335M	LCD_DATA1	-	R2	3.3V	lcd_data1	gpmc_a1	pr1_mii0_txen	ehrpwm2B	pr1_pru1_pru_r30_1	pr1_pru1_pru_r31_1	gpio2_7	
32	PWR	VIO_3P3	-	-	-								
33	335M	LCD_DATA2	-	R3	3.3V	lcd_data2	gpmc_a2	pr1_mii0_txd3	ehrpwm2_tripzone_input	pr1_pru1_pru_r30_2	pr1_pru1_pru_r31_2	gpio2_8	
34	PWR	VDD_BAT	-	-	-								

PIN	Class	Signal	PMIC Pin	AM3352 Pin	Domain Power	Option Signal0	Option Signal1	Option Signal2	Option Signal3	Option Signal4	Option Signal5	Option Signal6	Option Signal7
35	335M	LCD_DATA3	-	R4	3.3V	lcd_data3	gpmc_a3	pr1_mii0_txd2	ehrpwm0_synco	pr1_pru1_pru_r30_3	pr1_pru1_pru_r31_3	gpio2_9	
36	PM	PMIC_NRST	44	-	3.3V								
37	PWR	GND	-	-	-								
38	PWR	GND	-	-	-								
39	335M	LCD_DATA4	-	T1	3.3V	lcd_data4	gpmc_a4	pr1_mii0_txd1	eQEP2A_in	pr1_pru1_pru_r30_4	pr1_pru1_pru_r31_4	gpio2_10	
40	PWR	GND	-	-	-								
41	335M	LCD_DATA5	-	T2	3.3V	lcd_data5	gpmc_a5	pr1_mii0_txd0	eQEP2B_in	pr1_pru1_pru_r30_5	pr1_pru1_pru_r31_5	gpio2_11	
42	PWR	GND	-	-	-								
43	335M	LCD_DATA6	-	T3	3.3V	lcd_data6	gpmc_a6	pr1_edio_data_in6	eQEP2_index	pr1_edio_data_out6	pr1_pru1_pru_r30_6	pr1_pru1_pru_r31_6	gpio2_12
44	No Connect	NC1											
45	335M	LCD_DATA7	-	T4	3.3V	lcd_data7	gpmc_a7	pr1_edio_data_in7	eQEP2_strobe	pr1_edio_data_out7	pr1_pru1_pru_r30_7	pr1_pru1_pru_r31_7	gpio2_13
46	No Connect	NC2											
47	335M	LCD_DATA8	-	U1	3.3V	lcd_data8	gpmc_a12	ehrpwm1_tripzone_input	mcasp0_aclkx	uart5_txd	pr1_mii0_rxd3	uart2_ctsn	gpio2_14
48	No Connect	NC3											
49	335M	LCD_DATA9	-	U2	3.3V	lcd_data9	gpmc_a13	ehrpwm0_synco	mcasp0_fsx	uart5_rxd	pr1_mii0_rxd2	uart2_rtsn	gpio2_15
50	No Connect	NC4											
51	335M	LCD_DATA10	-	U3	3.3V	lcd_data10	gpmc_a14	ehrpwm1A	mcasp0_axr0	pr1_mii0_rxd1	uart3_ctsn	gpio2_16	
52	PM	PMIC_PBIN	25	-	3.3V								
53	335M	LCD_DATA11	-	U4	3.3V	lcd_data11	gpmc_a15	ehrpwm1B	mcasp0_ahclkr	mcasp0_axr2	pr1_mii0_rxd0	uart3_rtsn	gpio2_17
54	PWR	GND	-	-	-								
55	PWR	GND	-	-	-								
56	PWR	GND	-	-	-								
57	335M	LCD_DATA12	-	V2	3.3V	lcd_data12	gpmc_a16	eQEP1A_in	mcasp0_aclkr	mcasp0_axr2	pr1_mii0_rxlink	uart4_ctsn	gpio0_8
58	335M	GPMC_A0	-	R13	3.3V	gpmc_a0	gmii2_txen	rgmii2_tctl	rmii2_txen	gpmc_a16	pr1_mii_mt1_clk	ehrpwm1_tripzone_input	gpio1_16
59	335M	LCD_DATA13	-	V3	3.3V	lcd_data13	gpmc_a17	eQEP1B_in	mcasp0_fsr	mcasp0_axr3	pr1_mii0_rxer	uart4_rtsn	gpio0_9
60	335M	GPMC_A1	-	V14	3.3V	gpmc_a1	gmii2_rxdv	rgmii2_rctl	mmc2_dat0	gpmc_a17	pr1_mii1_txd3	ehrpwm0_synco	gpio1_17
61	335M	LCD_DATA14	-	V4	3.3V	lcd_data14	gpmc_a18	eQEP1_index	mcasp0_axr1	uart5_rxd	pr1_mii_mr0_clk	uart5_ctsn	gpio0_10
62	335M	GPMC_A2	-	U14	3.3V	gpmc_a2	gmii2_txd3	rgmii2_td3	mmc2_dat1	gpmc_a18	pr1_mii1_txd2	ehrpwm1A	gpio1_18
63	335M	LCD_DATA15	-	T5	3.3V	lcd_data15	gpmc_a19	eQEP1_strobe	mcasp0_ahclkx	mcasp0_axr3	pr1_mii0_rxdv	uart5_rtsn	gpio0_11
64	335M	GPMC_A3	-	T14	3.3V	gpmc_a3	gmii2_txd2	rgmii2_td2	mmc2_dat2	gpmc_a19	pr1_mii1_txd1	ehrpwm1B	gpio1_19
65	335M	LCD_PCLK	-	V5	3.3V	lcd_pclk	gpmc_a10	pr1_mii0_crs	pr1_edio_data_in4	pr1_edio_data_out4	pr1_pru1_pru_r30_10	pr1_pru1_pru_r31_10	gpio2_24
66	335M	GPMC_A4	-	R14	3.3V	gpmc_a4	gmii2_txd1	rgmii2_td1	rmii2_txd1	gpmc_a20	pr1_mii1_txd0	eQEP1A_in	gpio1_20
67	335M	LCD_VSYNC	-	U5	3.3V	lcd_vsync	gpmc_a8	gpmc_a13	pr1_edio_data_in2	pr1_edio_data_out2	pr1_pru1_pru_r30_8	pr1_pru1_pru_r31_8	gpio2_22
68	335M	GPMC_A5	-	V15	3.3V	gpmc_a5	gmii2_txd0	rgmii2_td0	rmii2_txd0	gpmc_a21	pr1_mii1_rxd3	eQEP1B_in	gpio1_21
69	335M	LCD_HSYNC	-	R5	3.3V	lcd_hsync	gpmc_a9	pr1_edio_data_in3	pr1_edio_data_out3	pr1_pru1_pru_r30_9	pr1_pru1_pru_r31_9	gpio2_23	
70	335M	GPMC_A6	-	U15	3.3V	gpmc_a6	gmii2_txclk	rgmii2_tclk	mmc2_dat4	gpmc_a22	pr1_mii1_rxd2	eQEP1_index	gpio1_22
71	335M	LCD_AC_BIAS_EN	-	R6	3.3V	lcd_ac_bias _en	gpmc_a11	pr1_mii1_crs	pr1_edio_data_in5	pr1_edio_data_out5	pr1_pru1_pru_r30_1 1	pr1_pru1_pru_r31_1 1	gpio2_25
72	335M	GPMC_A7	-	T15	3.3V	gpmc_a7	gmii2_rxclk	rgmii2_rclk	mmc2_dat5	gpmc_a23	pr1_mii1_rxd1	eQEP1_strobe	gpio1_23
73	PWR	GND	-	-	-								
74	PWR	GND	-	-	-								
75	335D	GPMC_AD0	-	U7	3.3V	gpmc_ad0							
76	335M	GPMC_A8	-	V16	3.3V	gpmc_a8	gmii2_rxd3	rgmii2_rd3	mmc2_dat6	gpmc_a24	pr1_mii1_rxd0	mcasp0_aclkx	gpio1_24

PIN	Class	Signal	PMIC Pin	AM3352 Pin	Domain Power	Option Signal0	Option Signal1	Option Signal2	Option Signal3	Option Signal4	Option Signal5	Option Signal6	Option Signal7
77	335D	GPMC_AD1	-	V7	3.3V	gpmc_ad1							
78	335M	GPMC_A9	-	U16	3.3V	gpmc_a9	gmii2_rxd2	rgmii2_rd2	mmc2_dat7/rmii2_crs_dv	gpmc_a25	pr1_mii_mr1_clk	mcasp0_fsx	gpio1_25
79	335D	GPMC_AD2	-	R8	3.3V	gpmc_ad2							
80	335M	GPMC_A10	-	T16	3.3V	gpmc_a10	gmii2_rxd1	rgmii2_rd1	rmii2_rxd1	gpmc_a26	pr1_mii1_rxdv	mcasp0_axr0	gpio1_26
81	335D	GPMC_AD3	-	T8	3.3V	gpmc_ad3							
82	335M	GPMC_A11	-	V17	3.3V	gpmc_a11	gmii2_rxd0	rgmii2_rd0	rmii2_rxd0	gpmc_a27	pr1_mii1_rxer	mcasp0_axr1	gpio1_27
83	335D	GPMC_AD4	-	U8	3.3V	gpmc_ad4							
84	335M	GPMC_CLK	-	V12	3.3V	gpmc_clk	lcd_memory_clk	gpmc_wait1	mmc2_clk	pr1_mii1_crs	pr1_mdio_mdclk	mcasp0_fsr	gpio2_1
85	335D	GPMC_AD5	-	V8	3.3V	gpmc_ad5							
86	335D	GPMC_BEN0_CLE	-	T6	3.3V	gpmc_be0n _cle							
87	335D	GPMC_AD6	-	R9	3.3V	gpmc_ad6							
88	335D	GPMC_ADVN_ALE	-	R7	3.3V	gpmc_advn _ale							
89	335D	GPMC_AD7	-	T9	3.3V	gpmc_ad7							
90	335D	GPMC_OEN_RE_N	-	T7	3.3V	gpmc_oen_ ren							
91	PWR	GND	-	-	-								
92	PWR	GND	-	-	-								
93	335M	GPMC_AD8	-	U10	VDDSHV2	gpmc_ad8	lcd_data23	mmc1_dat0	mmc2_dat4	ehrpwm2A	pr1_mii_mt0_clk	gpio0_22	
94	335M	GPMC_CSN3	-	T13	VDDSHV2	gpmc_csn3	gpmc_a3	rmii2_crs_dv	mmc2_cmd	pr1_mii0_crs	pr1_mdio_data	EMU4	gpio2_0
95	335M	GPMC_AD9	-	T10	VDDSHV2	gpmc_ad9	lcd_data22	mmc1_dat1	mmc2_dat5	ehrpwm2B	pr1_mii0_col	gpio0_23	
96	No Connect	NC5											
97	335M	GPMC_AD10	-	T11	VDDSHV2	gpmc_ad10	lcd_data21	mmc1_dat2	mmc2_dat6	ehrpwm2_tripzone_input	pr1_mii0_txen	gpio0_26	
98	335D	GPMC_WE_N	-	U6	3.3V	gpmc_wen							
99	335M	GPMC_AD11	-	U12	VDDSHV2	gpmc_ad11	lcd_data20	mmc1_dat3	mmc2_dat7	ehrpwm0_synco	pr1_mii0_txd3	gpio0_27	
100	335D	GPMC_WAIT0	-	T17	3.3V	gpmc_wait0							
101	335M	GPMC_AD12	-	T12	VDDSHV2	gpmc_ad12	lcd_data19	mmc1_dat4	mmc2_dat0	eQEP2A_in	pr1_mii0_txd2	pr1_pru0_pru_r30_14	gpio1_12
102	335M	GPMC_BEN1	-	U18	3.3V	gpmc_be1n	gmii2_col	gpmc_csn6	mmc2_dat3	gpmc_dir	pr1_mii1_rxlink	mcasp0_aclkr	gpio1_28
103	335M	GPMC_AD13	-	R12	VDDSHV2	gpmc_ad13	lcd_data18	mmc1_dat5	mmc2_dat1	eQEP2B_in	pr1_mii0_txd1	pr1_pru0_pru_r30_15	gpio1_13
104	335D	GPMC_WP_N	-	U17	3.3V	gpmc_wpn							
105	335M	GPMC_AD14	-	V13	VDDSHV2	gpmc_ad14	lcd_data17	mmc1_dat6	mmc2_dat2	eQEP2_index	pr1_mii0_txd0	pr1_pru0_pru_r31_14	gpio1_14
106	No Connect	NC6											
107	335M	GPMC_AD15	-	U13	VDDSHV2	gpmc_ad15	lcd_data16	mmc1_dat7	mmc2_dat3	eQEP2_strobe	pr1_ecap0_ecap_capin_apwm_o	pr1_pru0_pru_r31_15	gpio1_15
108	No Connect	NC7											
109	PWR	GND	-	-	-								
110	PWR	GND	-	-	-								
111	335M	GPMC_CSN2	-	V9	3.3V	gpmc_csn2	gpmc_be1n	mmc1_cmd	pr1_edio_data_in7	pr1_edio_data_out7	pr1_pru1_pru_r30_13	pr1_pru1_pru_r31_13	gpio1_31
112	335M	GMII1_RXD0	-	M16	3.3V	gmii1_rxd0	rmii1_rxd0	rgmii1_rd0	mcasp1_ahclkx	mcasp1_ahclkr	mcasp1_aclkr	mcasp0_axr3	gpio2_21
113	335M	GPMC_CSN1	-	U9	3.3V	gpmc_csn1	gpmc_clk	mmc1_clk	pr1_edio_data_in6	pr1_edio_data_out6	pr1_pru1_pru_r30_12	pr1_pru1_pru_r31_12	gpio1_30
114	335M	GMII1_RXD1	-	L15	3.3V	gmii1_rxd1	rmii1_rxd1	rgmii1_rd1	mcasp1_axr3	mcasp1_fsr	eQEP0_strobe	mmc2_clk	gpio2_20
115	335D	USB0_VBUS	-	P15	USB0_VBUS								
116	335M	GMII1_RXD2	-	L16	3.3V	gmii1_rxd2	uart3_txd	rgmii1_rd2	mmc0_dat4	mmc1_dat3	uart1_rin	mcasp0_axr1	gpio2_19
117	335D	USB0_ID	-	P16	USB0_ID								
118	335M	GMII1_RXD3	-	L17	3.3V	gmii1_rxd3	uart3_rxd	rgmii1_rd3	mmc0_dat5	mmc1_dat2	uart1_dtrn	mcasp0_axr0	gpio2_18

PIN	Class	Signal	PMIC Pin	AM3352 Pin	Domain Power	Option Signal0	Option Signal1	Option Signal2	Option Signal3	Option Signal4	Option Signal5	Option Signal6	Option Signal7
119	335D	USB1_VBUS	-	T18	USB1_VBUS								
120	335M	GMII1_RXCLK	-	L18	3.3V	gmii1_rxclk	uart2_txd	rgmii1_rclk	mmc0_dat6	mmc1_dat1	uart1_dsrn	mcasp0_fsx	gpio3_10
121	335D	USB1_DP	-	R17	USB1_DP								
122	335M	GMII1_RXDV	-	J17	3.3V	gmii1_rxdv	lcd_memory_clk	rgmii1_rctl	uart5_txd	mcasp1_aclkx	mmc2_dat0	mcasp0_aclkr	gpio3_4
123	335D	USB1_DM	-	R18	USB1_DM								
124	No Connect	NC8											
125	335D	USB1_CE	-	P18	USB1_CE								
126	335M	GMII1_TXCLK	-	K18	3.3V	gmii1_txclk	uart2_rxd	rgmii1_tclk	mmc0_dat7	mmc1_dat0	uart1_dcdn	mcasp0_aclkx	gpio3_9
127	PWR	GND	-	-	-								
128	335M	GMII1_TXD0	-	K17	3.3V	gmii1_txd0	rmii1_txd0	rgmii1_td0	mcasp1_axr2	mcasp1_aclkr	eQEP0B_in	mmc1_clk	gpio0_28
129	335D	USB1_ID	-	P17	USB1_ID								
130	335M	GMII1_TXD1	-	K16	3.3V	gmii1_txd1	rmii1_txd1	rgmii1_td1	mcasp1_fsr	mcasp1_axr1	eQEP0A_in	mmc1_cmd	gpio0_21
131	335D	USB0_DM	-	N18	USB0_DM								
132	335M	GMII1_TXD2	-	K15	3.3V	gmii1_txd2	dcan0_rx	rgmii1_td2	uart4_txd	mcasp1_axr0	mmc2_dat2	mcasp0_ahclkx	gpio0_17
133	335D	USB0_DP	-	N17	USB0_DP								
134	335M	GMII1_TXD3	-	J18	3.3V	gmii1_txd3	dcan0_tx	rgmii1_td3	uart4_rxd	mcasp1_fsx	mmc2_dat1	mcasp0_fsr	gpio0_16
135	335D	USB0_CE	-	M15	USB0_CE								
136	335M	GMII1_TXEN	-	J16	3.3V	gmii1_txen	rmii1_txen	rgmii1_tctl	timer4	mcasp1_axr0	eQEP0_index	mmc2_cmd	gpio3_3
137	335M	USB1_DRVVBUS	-	F15	3.3V	USB1_DRVVBUS	gpio3_13						
138	335M	GMII1_COL	-	H16	3.3V	gmii1_col	rmii2_refclk	spi1_sclk	uart5_rxd	mcasp1_axr2	mmc2_dat3	mcasp0_axr2	gpio3_0
139	335M	USB0_DRVVBUS	-	F16	3.3V	USB0_DRVVBUS	gpio0_18						
140	No Connect	NC9											
141	335M	MDC	-	M18	3.3V	mdio_clk	timer5	uart5_txd	uart3_rtsn	mmc0_sdwp	mmc1_clk	mmc2_clk	gpio0_1
142	No Connect	NC10											
143	335M	MDIO	-	M17	3.3V	mdio_data	timer6	uart5_rxd	uart3_ctsn	mmc0_sdcd	mmc1_cmd	mmc2_cmd	gpio0_0
144	335M	MCASP0_AXR1	-	D13	3.3V	mcasp0_axr1	eQEP0_index	mcasp1_axr0	EMU3	pr1_pru0_pru_r30_6	pr1_pru0_pru_r31_6	gpio3_20	
145	335M	RMII1_REFCLK	-	H18	3.3V	rmii1_refclk	xdma_event_intr2	spi1_cs0	uart5_txd	mcasp1_axr3	mmc0_pow	mcasp1_ahclkx	gpio0_29
146	PWR	GND	-	-	-								
147	335M	GMII1_CRS	-	H17	3.3V	gmii1_crs	rmii1_crs_dv	spi1_d0	I2C1_SDA	mcasp1_aclkx	uart5_ctsn	uart2_rxd	gpio3_1
148	335M	MCASP0_FSR	-	C13	3.3V	mcasp0_fsr	eQEP0B_in	mcasp0_axr3	mcasp1_fsx	EMU2	pr1_pru0_pru_r30_5	pr1_pru0_pru_r31_5	gpio3_19
149	335M	GMII1_RXERR	-	J15	3.3V	gmii1_rxerr	rmii1_rxerr	spi1_d1	I2C1_SCL	mcasp1_fsx	uart5_rtsn	uart2_txd	gpio3_2
150	335M	MCASP0_ACLKR	-	B12	3.3V	mcasp0_aclkr	eQEP0A_in	mcasp0_axr2	mcasp1_aclkx	mmc0_sdwp	pr1_pru0_pru_r30_4	pr1_pru0_pru_r31_4	gpio3_18
151	335M	MMC0_CMD	-	G18	VDDSHV4	mmc0_cmd	gpmc_a25	uart3_rtsn	uart2_txd	dcan1_rx	pr1_pru0_pru_r30_13	pr1_pru0_pru_r31_13	gpio2_31
152	335M	MCASP0_ACLKX	-	A13	3.3V	mcasp0_aclkx	ehrpwm0A	spi1_sclk	mmc0_sdcd	pr1_pru0_pru_r30_0	pr1_pru0_pru_r31_0	gpio3_14	
153	335M	MMC0_CLK	-	G17	VDDSHV4	mmc0_clk	gpmc_a24	uart3_ctsn	uart2_rxd	dcan1_tx	pr1_pru0_pru_r30_12	pr1_pru0_pru_r31_12	gpio2_30
154	335M	MCASP0_AHCLKX	-	A14	3.3V	mcasp0_ahc lkx	eQEP0_stro be	mcasp0_axr3	mcasp1_axr1	EMU4	pr1_pru0_pru_r30_7	pr1_pru0_pru_r31_7	gpio3_21
155	335M	MMC0_DAT0	-	G16	VDDSHV4	mmc0_dat0	gpmc_a23	uart5_rtsn	uart3_txd	uart1_rin	pr1_pru0_pru_r30_11	pr1_pru0_pru_r31_11	gpio2_29
156	335M	MCASP0_AHCLKR	-	C12		mcasp0_ahclkr	ehrpwm0_synci	mcasp0_axr2	spi1_cs0	eCAP2_in_PWM2_out	pr1_pru0_pru_r30_3	pr1_pru0_pru_r31_3	gpio3_17
157	335M	MMC0_DAT1	-	G15	VDDSHV4	mmc0_dat1	gpmc_a22	uart5_ctsn	uart3_rxd	uart1_dtrn	pr1_pru0_pru_r30_10	pr1_pru0_pru_r31_10	gpio2_28
158	335D	WARMRST_N	-	A10	3.3V	nRESETIN_OUT							
159	335M	MMC0_DAT2	-	F18	VDDSHV4	mmc0_dat2	gpmc_a21	uart4_rtsn	timer6	uart1_dsrn	pr1_pru0_pru_r30_9	pr1_pru0_pru_r31_9	gpio2_27
160	335M	EMU0	-	C14	3.3V	EMU0	gpio3_7						

PIN	Class	Signal	PMIC Pin	AM3352 Pin	Domain Power	Option Signal0	Option Signal1	Option Signal2	Option Signal3	Option Signal4	Option Signal5	Option Signal6	Option Signal7
161	335M	MMC0_DAT3	-	F17	VDDSHV4	mmc0_dat3	gpmc_a20	uart4_ctsn	timer5	uart1_dcdn	pr1_pru0_pru_r30_8	pr1_pru0_pru_r31_8	gpio2_26
162	335M	EMU1	-	B14	3.3V	EMU1	gpio3_8						
163	PWR	GND	-	-	-								
164	PWR	GND	-	-	-								
165	335M	UART0_CTSN	-	E18	3.3V	uart0_ctsn	uart4_rxd	dcan1_tx	I2C1_SDA	spi1_d0	timer7	pr1_edc_sync0_out	gpio1_8
166	335D	TCK	-	A12	3.3V	TCK							
167	335M	UART0_RTSN	-	E17	3.3V	uart0_rtsn	uart4_txd	dcan1_rx	I2C1_SCL	spi1_d1	spi1_cs0	pr1_edc_sync1_out	gpio1_9
168	335D	TDI	-	B11	3.3V	TDI							
169	335M	UART0_TXD	-	E16	3.3V	uart0_txd	spi1_cs1	dcan0_rx	I2C2_SCL	eCAP1_in_PWM1_out	pr1_pru1_pru_r30_15	pr1_pru1_pru_r31_15	gpio1_11
170	335D	TDO	-	A11	3.3V	TDO							
171	335M	UART0_RXD	-	E15	3.3V	uart0_rxd	spi1_cs0	dcan0_tx	I2C2_SDA	eCAP2_in_PWM2_out	pr1_pru1_pru_r30_14	pr1_pru1_pru_r31_14	gpio1_10
172	335D	TMS	-	C11	3.3V	TMS							
173	335M	UART1_RXD	-	D16	3.3V	uart1_rxd	mmc1_sdwp	dcan1_tx	I2C1_SDA	pr1_uart0_rxd	pr1_pru1_pru_r31_16	gpio0_14	
175	335M	UART1_TXD	-	D15	3.3V	uart1_txd	mmc2_sdwp	dcan1_rx	I2C1_SCL	pr1_uart0_txd	pr1_pru0_pru_r31_16	gpio0_15	
176	PWR	VREFN	-	A9	1.8V	VREFN							
177	335M	UART1_CTSN	-	D18	3.3V	uart1_ctsn	timer6	dcan0_tx	I2C2_SDA	spi1_cs0	pr1_uart0_cts_n	pr1_edc_latch0_in	gpio0_12
178	PWR	VREFP	-	B9	1.8V	VREFP							
179	335M	UART1_RTSN	-	D17	3.3V	uart1_rtsn	timer5	dcan0_rx	I2C2_SCL	spi1_cs1	pr1_uart0_rts_n	pr1_edc_latch1_in	gpio0_13
180	No Connect	NC12											
181	PWR	GND	-	-	-								
182	PWR	GND	-	-	-								
183	335M	SPI0_D0	-	B17	3.3V	spi0_d0	uart2_txd	I2C2_SCL4	ehrpwm0B	pr1_uart0_rts_n	pr1_edio_latch_in	EMU3	gpio0_3
184	335D	AIN0	-	B6	1.8V	AIN0							
185	335M	SPI0_D1	-	B16	3.3V	spi0_d1	mmc1_sdwp	I2C1_SDA4	ehrpwm0_tripzone_input	pr1_uart0_rxd	pr1_edio_data_in0	pr1_edio_data_out0	gpio0_4
186	335D	AIN1	-	C7	1.8V	AIN1							
187	335M	SPI0_SCLK	-	A17	3.3V	spi0_sclk	uart2_rxd	I2C2_SDA4	ehrpwm0A	pr1_uart0_cts_n	pr1_edio_sof	EMU2	gpio0_2
188	335D	AIN2	-	B7	1.8V	AIN2							
189	335M	SPI0_CS1	-	C15	3.3V	spi0_cs1	uart3_rxd	eCAP1_in_PWM1_out	mmc0_pow	xdma_event_intr2	mmc0_sdcd	EMU4	gpio0_6
190	335D	AIN3	-	A7	1.8V	AIN3							
191	335M	SPI0_CS0	-	A16	3.3V	spi0_cs0	mmc2_sdwp	I2C1_SCL4	ehrpwm0_synci	pr1_uart0_txd	pr1_edio_data_in1	pr1_edio_data_out1	gpio0_5
192	335D	AIN4	-	C8	1.8V	AIN4							
193	335M	SPI1_SCLK	-	C18	3.3V	eCAP0_in_PWM0_out	uart3_txd	spi1_cs1	pr1_ecap0_ecap_capin_apwm_o	spi1_sclk	mmc0_sdwp	xdma_event_intr2	pio0_7
194	335D	AIN5	-	B8	1.8V	AIN5							
195	335M	SPI1_D0_MOSI	-	B13	3.3V	mcasp0_fsx	ehrpwm0B	spi1_d0	mmc1_sdcd	pr1_pru0_pru_r30_1	pr1_pru0_pru_r31_1	gpio3_15	
196	335D	AIN6	-	A8	1.8V	AIN6							
197	335M	SPI1_D1_MISO	-	D12	3.3V	mcasp0_axr0	ehrpwm0_tripzone_input	spi1_d1	mmc2_sdcd	pr1_pru0_pru_r30_2	pr1_pru0_pru_r31_2	gpio3_16	
198	335D	AIN7	-	C9	1.8V	AIN7							
199	PWR	GND	-	-	-								
200	PWR	GND	-	-	-								
201	335M	XDMA_EVENT_INR1	-	D14	3.3V	xdma_event _intr1	tclkin	clkout2	timer7	pr1_pru0_pru_r31_1 6	EMU3	gpio0_20	
202	PWR	AGND	-	-	-								
203	335M	XDMA_EVENT_INR0	-	A15	3.3V	xdma_event _intr0	timer4	clkout1	spi1_cs1	pr1_pru1_pru_r31_1 6	EMU2	gpio0_19	
204	PWR	AGND											

7.2 Mechanical Drawings